OPTi-DXBB PC/AT Chipset (82C496/82C206)

Preliminary

82C496 DATA BOOK

Version 1.2

Disclaimer

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1.0 FEATURES

The OPTi-DXBB is a two-chip solution providing optimal performance for 486DX, 386DX and 486SX/487SX based AT systems. The OPTi-DXBB is designed for systems running at frequencies of 20, 25, 33 and up to 40 Mhz. It includes the 82C496 System/Data Controller and the 82C206 Integrated Peripheral Controller (IPC). Refer to the data book supplied by your third-party source for information on the 82C206.

The 82C496 System Controller integrates a single chip CPU interface controller, DRAM controller and AT bus controller. It is featured as a low-cost, cacheless solution with minimal performance degradation when compared with cache-based, high performance systems. It also provides easy hooks for external cache controllers and high performance local-bus peripherals. By combining the 82C496 with a standard 82C206, a modularized, upgradable system can easily be implemented.

Features

The OPTi-DXBB features include:

- o Modular design is simplified by using the same chipset for 386DX, 486SX, 486DX and 487SX systems
- o One 184-pin CMOS Plastic Flat Package (PFP), and one 84-pin PLCC
- o Supports 3,2,2,2 cache DRAM burst cycles for 486 bsed system
- o Supports up to 64-MB of high speed local memory
- o Support s 256K, 1M and 4 M DRAM with two-way page mode operation
- o Provides programmable control of two non-cacheable regions
- o Shadow RAMs support
- o Optional caching of shadowed Video BIOS
- o Transparent 8042 keyboard emulation for Fast CPU reset and GATEA20 generation
- o Hardware support for Turbo mode
- o Selectable AT bus clock of CLK2IN/4, CLK2IN/5, CLK2IN/6 or CLK2IN/8
- o 0 or 1 wait state options for 16-bit AT bus cycles
- o Slow refresh available for laptop applications
- o Hidden refresh to boost CPU bandwidth
- o CAS# before RAS# refresh reduces power consumption
- o WEITEK 3167/4167 coprocessor support
- o High performance local bus device support

FUNCTIONAL BLOCKS:

The following functional blocks are integrated into the 82C496:

1. Clock generator logic
2. Reset logic
3. Numerical Processor glue logic
4. AT bus interface logic
5. CPU interface & control
6. Port B and NMI logic
7. Data assembly/disassembly logic for ISA/DMA master access
8. Fast CPU warm reset and gated A20 control
9. Decodes for keyboard controller, RTC and ROM BIOS
10. DRAM interface control and interface
11. 486 burst mode logic
12. 386 pipeline mode support
13. External cache system and local device interface logic
14. CPU special cycles control

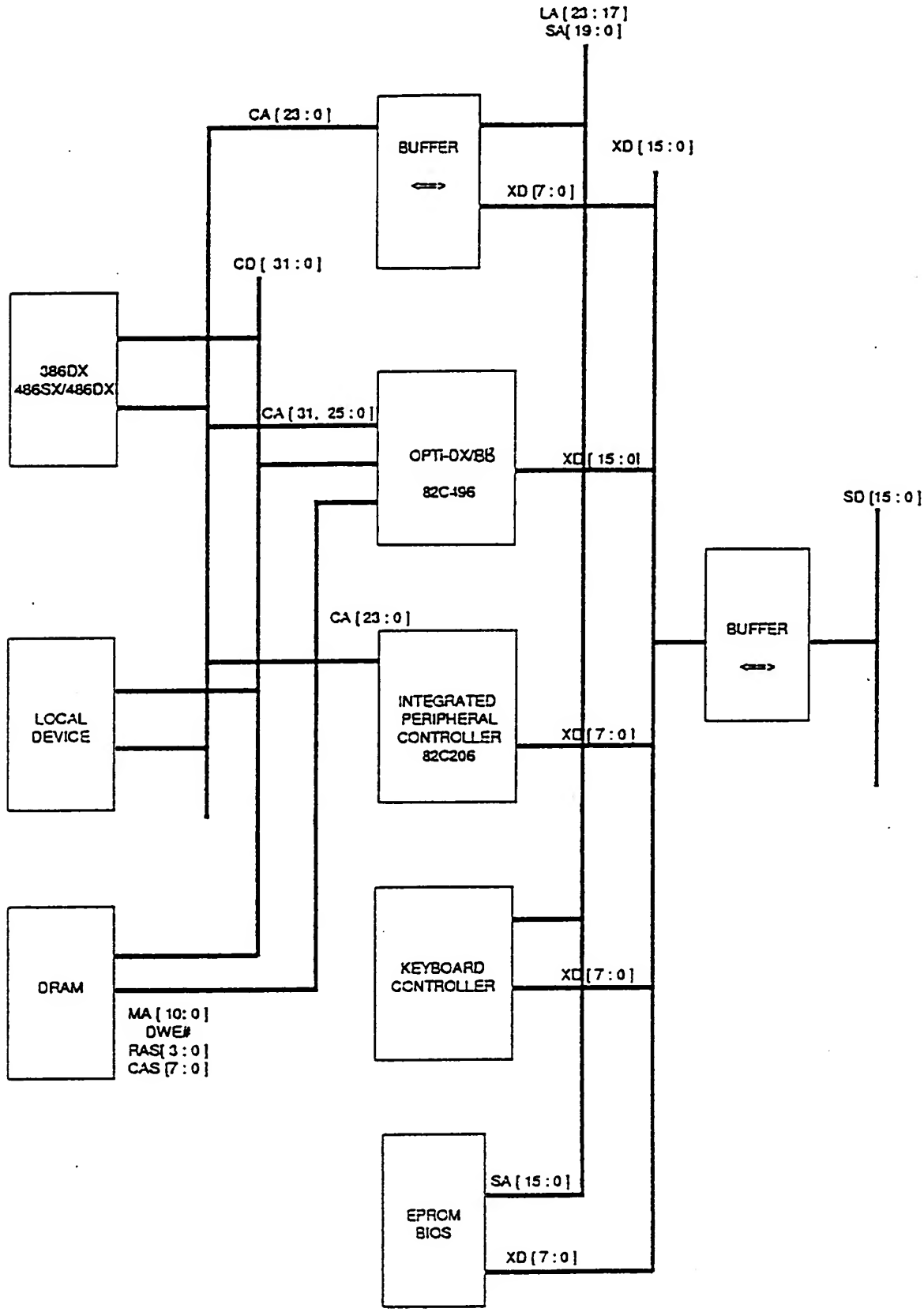


Figure1 OPTi - DX/BB SYSTEM BLOCK DIAGRAM

2.0 CONFIGURATION REGISTER DESCRIPTION:

The DXBB consists of eleven configuration registers. An indexing scheme is used to access these registers. Port 22h is used as an index register and port 24h is used as a data port. Each access to a configuration register consists of a write to port 22h, specifying the desired register in the data byte, followed by a read or write to port 24h, with the actual register data. Every access to a configuration register must be preceded by a write to port 22h even if the same register is being accessed. All reserved bits are set to zero by default and must be set to zero to ensure future compatibility.

Register I
Index: 30h

Revision / DRAM Type

BIT	FUNCTION	DEFAULT
7-6	Revision number	00
5	Reserved	0
4-0	DRAM type used. See the following table	11111

BIT 4 3 2 1 0	BANK 0	BANK 1	BANK 2	BANK 3	TOTAL
11111	256K	X	X	X	1M
00001	256K	256K	X	X	2M
00010	256K	1M	X	X	5M
00011	256K	256K	1M	X	6M
00100	256K	1M	1M	X	9M
00101	256K	256K	1M	1M	10M
00110	256K	1M	1M	1M	13M
00111	1M	X	X	X	4M
01000	1M	1M	X	X	8M
01001	1M	1M	1M	X	12M
01010	1M	1M	1M	1M	16M
01011	1M	1M	4M	X	24M
01100	1M	1M	4M	4M	40M
01101	4M	X	X	X	16M
01110	4M	4M	X	X	32M
01111	4M	4M	4M	X	48M
00000	4M	4M	4M	4M	64M

Register II
Index: 31h

DRAM Control Register

BIT	FUNCTION	DEFAULT
7	Hidden Refresh Control. 0 =enable , 1=disable Note: for 386 systems running in pipeline mode (non-cache), Hidden Refresh should be disabled.	1
6	Slow Refresh Control. 0 = enable , 1 = disable	0
5	Parity Check Enable. 0 =disable, 1 =enable	0
4	Reserved	0
3-2	DRAM write cycle wait states 00 0 wait state 01 1 wait state 10 2 wait states 11 3 wait states	11
1-0	DRAM read cycle wait states: 00 0 wait state 01 1 wait state 10 2 wait states 11 3 wait states	11

Register III
Index: 32h

Shadow Register #1

BIT	FUNCTION	DEFAULT
7	Shadow RAM at F0000h-FFFFFh area 0 = Shadow RAM enable and RAM is write-protected, 1 =disable, read from ROM, write to DRAM (if 34h<1> = 0) read /write is directed to ROM (if 34h<1> = 1)	1
6	Shadow RAM at E0000h-EFFFFh Area. 0 =disable, 1 =enable	1
5	Shadow RAM at D0000h-DFFFFh Area. 0 =disable, 1 =enable	1
4	Shadow RAM at C0000h-CFFFFh Area. 0 =disable, 1 =enable. If disabled, ROMCS# is generated	1
3	Shadow RAM copy enable for address area C0000h-EFFFFh 0 =Read/Write at AT bus 1 =Read from AT bus and write into shadow RAM	0
2	Shadow RAM write protect at address area E0000h-EFFFFh 0 =Write Protect Disable, 1 =Write Protect Enable	0
1	Shadow RAM write protect at address area D0000h-DFFFFh 0 =Write Protect Disable, 1 =Write Protect Enable	0
0	Shadow RAM write protect at address area C0000h-CFFFFh 0 =Write Protect Disable, 1 =Write Protect Enable	0

Register IV
Index: 33h

Shadow Register #2

BIT	FUNCTION	DEFAULT
7	Enable Shadow RAM at EC000h-EFFFFh area 0 =disable, 1 =enable	0
6	Enable Shadow RAM at E8000h-EBFFFh area 0 =disable, 1 =enable	0
5	Enable Shadow RAM at E4000h-E7FFFh area 0 =disable, 1 =enable	0
4	Enable Shadow RAM at E0000h-E3FFFh area 0 =disable, 1 =enable	0
3	Enable Shadow RAM at DC000h-DFFFFh area 0 =disable, 1 =enable	0
2	Enable Shadow RAM at D8000h-DBFFFh area 0 =disable, 1 =enable	0
1	Enable Shadow RAM at D4000h-D7FFFh area 0 =disable, 1 =enable	0
0	Enable Shadow RAM at D0000h-D3FFFh area 0 =disable, 1 =enable	0

Register V
Index: 34h

Shadow Register #3

BIT	FUNCTION	DEFAULT
7	Enable Shadow RAM at CC000h-CFFFFh area 0 =disable, 1 =enable	0
6	Enable Shadow RAM at C8000h-CBFFFh area 0 =disable, 1 =enable	0
5	Enable Shadow RAM at C4000h-C7FFFh area 0 =disable, 1 =enable	0
4	Enable Shadow RAM at C0000h-C3FFFh area 0 =disable, 1 =enable	0
3-2	Reserved	00
1	ROM F0000h-FFFFFh area write enable 0 =disable, and data is written into DRAM, 1 =enable, SMEM# command is generated	0
0	Video BIOS at C0000h-C8000h area non-cachable 1 =cachable, 0 =Non-cachable	0

Register VI
Index: 35h

Remap Register

BIT	FUNCTION	DEFAULT
7-6	Reserved	00
5-0	Remap area control of address bits of A25 to A20 000000 =No Mapping, 000001 =1M, 000010 =2M etc. till 63M	000000

Register VII
Index: 36h

AT Control Register #1

BIT	FUNCTION	DEFAULT
7	Reserved	0
6	Keyboard and Fast Reset control. When this bit is enabled, a "HALT" instruction is required before a CPU reset can be generated. 0 =enable, 1 =disable	0
5	Master mode byte swap enable. 0 =disable, 1 =enable	0
4	Always non-cachable for whole memory area when enabled. 0 =disable, 1 =enable	0
3	Generate a single ALE instead of multiple ALEs during a bus conversion cycle. 0 =disable, 1 =enable	0
2	Extra AT cycle wait state enable. 0 =0 wait state, 1 =1 wait state	0
1-0	AT bus clock selection. AT CLOCK = CLK2IN/4, CLK2IN/5, CLK2IN/6 or CLK2IN/8, if bit 0 and bit 1 = 11, 10, 01, or 00 respectively.	00

Register VIII
Index: 37h

Non-Cacheable Area 0 - Register 1

BIT	FUNCTION	DEFAULT
7	Reserved	0
6-4	Size of non-cachable memory block 1. 000 = 64K 001 = 128K 010 = 256K 011 = 512K 100 = 2M 101 = 4M 110 = 8M 111 = disable	111
3-2	Reserved	00
1-0	Address bit A25 and A24 of non-cachable memory block 1. These two bits are always valid no matter what the size of non-cachable block is.	X

Register IX
Index: 38h

Non-Cacheable Area 0 - Register 2

BIT	FUNCTION	DEFAULT
7-0	Address bit A23-A16 of non-cachable memory block 1.	X

Valid Starting Address Bits vs Non-cachable Block Size
v = Valid Bit
x = Don't Care

Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	v	v	v	v	v	v	v	v
128K	v	v	v	v	v	v	v	x
256K	v	v	v	v	v	v	x	x
512K	v	v	v	v	v	x	x	x
2M	v	v	v	x	x	x	x	x
4M	v	v	x	x	x	x	x	x
8M	v	x	x	x	x	x	x	x

Register X
Index: 39h

Non-Cacheable Area 1 - Register 1

BIT	FUNCTION	DEFAULT
7	Reserved	0
6-4	Size of non-cachable memory block 2. 000 = 64K 001 = 128K 010 = 256K 011 = 512K 100 = 2M 101 = 4M 110 = 8M 111 = disable	111
3-2	Reserved	00
1-0	Address bit A25 and A24 of non-cachable memory block 2. These two bits are always valid no matter what the size of non-cachable block is.	X

Register XI
Index: 3Ah

Non-Cacheable Area 1 - Register 2

BIT	FUNCTION	DEFAULT
7-0	Address bit A23-A16 of non-cachable memory block 2.	X

Valid Starting Address Bits vs Non-cachable Block Size
v = Valid Bit
x = Don't Care

Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	v	v	v	v	v	v	v	v
128K	v	v	v	v	v	v	v	x
256K	v	v	v	v	v	v	x	x
512K	v	v	v	v	v	x	x	x
2M	v	v	v	x	x	x	x	x
4M	v	v	x	x	x	x	x	x
8M	v	x	x	x	x	x	x	x

PORT 60h

Port 60h and 64h emulate the registers of a keyboard controller, allowing the generation of the fast GATEA20 and CPURST signals. The sequence is software transparent and requires no BIOS modification. The fast GATEA20 generation sequence involves writing data D1h to port 64h, then writing data 02h to port 60h. A write to port 64h with data D0h will enable the status of GATEA20(bit 1 of port 60h) and the system reset (bit 0 of port 60h) to be readable.

PORT 61h(Port B)

BIT	FUNCTION	R/W
7	System parity check	Read only
6	IO Channel check	Read only
5	Timer OUT2 detect	Read only
4	Refresh detect	Read only
3	IO Channel check enable: 0=enable, 1=disable	R/W
2	Parity check enable: 0 =enable, 1=disable	R/W
1	Speaker output enable: 1 =enable, 0=disable	R/W
0	Timer 2 gate 1 =enable, 0 =disable	R/W

PORT 64h

Emulate keyboard controller CPU warm reset function. A port 64h write cycle with data FEh will generate a reset pulse to CPU.

PORT 70h

NMI is enabled when bit 7 =0.

3.0 82C496 PIN DESCRIPTIONS

3.1 CLOCKs & RESETs

Name	Type	Pin No.	Description
PWRGD#	I	38	***Power Good.*** This input reflects the "Wire-OR" status of the external reset switch and the power supply PWRGD signal. This signal must be low for normal operation.
CPURST	O	165	***CPU Reset.*** When active (high), this signal resets the CPU. CPURST is active in response to SYSRST#, fast CPU Reset emulation and CPU shutdown cycles.
SYSRST#	O	56	***System Reset.*** This active low signal is used as a system level reset output in response to the PWRGD# signal. It resets motherboard peripherals and is externally buffered and inverted to provide the RSTDRV function on the AT bus.
ECLK	I	2	***Early Clock.*** Half the frequency of CLK2, this input is used as the phase reference for the internal state machines. ECLK matches the CPU's rated frequency. It is equal to the CPU clock for 486 systems and is half the CPU clock for 386 systems.
CLK2	I	183	***Clock2.*** Crystal oscillator input which has a frequency twice the rated CPU clock (and twice ECLK). This signal is used as clock source for the internal state machines and for the generation of CPURST.
ATCLK	O	91	***AT Bus Clock.*** This output is derived by dividing the CLK2 input by the appropriate amount specified in the AT control register (Reg36h<1:0>). Possible settings include: CLK2/4, CLK2/5, CLK2/6 or CLK2/8. ATCLK is externally buffered before being connected to the AT bus.
OSC	I	94	***Oscillator.*** This 14.31818 MHz oscillator input monitors the AT bus oscillator frequency. It provides the timing reference for the OSC12 output.
OSC12	O	95	***Oscillator Divided by 12.*** OSC is internally divided by 12 to provide this 1.19MHz output for the RTC.

3.2 CPU INTERFACE

Name	Type	Pin No.	Description
PREQI/BLST#	I	180	***Numeric Processor Extension Request*** (386 mode) or ***Burst Last*** (486 mode). For 386 systems, this is the PEREQ signal from the coprocessor indicating that it has operands ready to transfer. For 486 systems, this is the BLAST# signal from the CPU indicating the last transfer in a burst operation.
PREQO/BRDY#	O	167	***Numeric Processor Extension Request Output*** (386 mode) or ***Burst Ready*** (486 mode). For 386 systems, this signal drives the CPU's PEREQ input. For 486 systems, this signal drives the CPU's BRDY# input.
A31 A[25:17], A[7:2]	I	124 122-117, 114-112, 102-97	***CPU Address bus.*** Address lines A31, A25-A17, A7-A2
A[16:8]	B	111-107, 105,106, 104,103	***CPU Address bus.*** Address lines A16-A8 are input signals except during DMA cycles. A[16:9] become outputs and convey DMA address 16-9 for 16-bit DMA cycles. A[15:8] become outputs and convey DMA address 15-8 for 8-bit DMA cycles.
DRAMS#	I	123	***DRAM Status.*** A status signal to indicate CPU address lines A[30:26] are low . DRAMS# must be asserted (low) to enable the DRAM controller. This pin can be used to support multiple DXBB system and data controllers.
BE[3:0]#	B	168-171	***Byte Enables 3-0.*** These four signals define the byte(s) involved in a data transfer. They are inputs for CPU cycles and outputs for Master and DMA cycles.
NA#/KEN#	O	164	***Next Address*** (386 mode) or ***Cache Enable*** (486 mode). In 386 mode this signal is connected to the CPU's NA# pin to request pipelined addressing. for local memory cycles (it is deactivated for Numeric Coprocessor and AT bus cycles). In 486 mode, it is connected to KEN# of the 486 and becomes active when a cacheable memory area is detected.
ADS#	I	176	***Address Status.*** Input from CPU to indicate a valid address is present on the bus.
W/R#	I	179	***Write / Read.*** Input from CPU, used along with D/C#, M/IO# and BE[3:0]# to decode cycle type in progress.
D/C#	I	178	***Data / Control.*** Input from CPU, used along with W/R#, M/IO# and BE[3:0]# to decode cycle type in progress.
M/IO#	I	177	***Memory / IO.*** Input from CPU, used along with W/R#,D/C# and BE[3:0]# to decode cycle type in progress.
RDY#	B	166	***Ready.*** As an output, it is driven to the CPU to terminate a bus cycle. If a local device is detected and RDYI# is inactive, then RDY# becomes an input.
LDEV#	I	5	***Local Device.*** Local devices drive this input to indicate they are responding to the current cycle.
RDYI#	I	6	***Coprocessor Ready Input.*** This input is driven by the coprocessor's READYO# pin and is synchronized before being sent to the CPU on the RDY# line.

TURBO	I	3	*Turbo Mode Selection.* Normal (Turbo) mode is maintained when this pin is asserted (high). Non-Turbo mode is entered when this pin is deasserted by keeping the CPU in its hold state for approximately two thirds of the time. The refresh request signal is used as the clock source to control the hold duty cycle.
LD[31:0]	B	125-128, 130-137, 140-148, 150-160	*CPU Data Bus.* 32-bit wide data bus organized as four bytes.

3.3 NUMERICAL PROCESSOR INTERFACE

Name	Type	Pin No	Description
NPERR#	I	182	*Numeric Coprocessor Error.* This input is driven by a coprocessor to indicate an error condition when an unmasked exception occurs. It is used internally to generate NPINT and BUSY# (386 mode) to the CPU. Additionally, if active after a reset, it indicates the presence of a coprocessor.
NPBSY#	I	181	*Numeric Coprocessor Busy and 386/486# strapping option.* This input is sampled during a system reset to determine the processor type installed (386 or 486). 486 systems should tie this input low and 386 systems should provide an external pull-up. For 386 systems, this input is also connected to the coprocessor's BUSY# output and is used internally to generate NPINT and BUSY# to the CPU.
BUSY#/ IGNNE#	O	173	*386 Busy* (386 mode) or *Ignore Numeric Coprocessor Error* (486 mode). In 386 mode, this signal is active when the coprocessor is busy or a coprocessor error has occurred. It is also toggled if a coprocessor is not installed and the CPU issues a coprocessor instruction. In 486 mode, this output tells the CPU to ignore the numeric coprocessor's error output.
NPRST/EADS#	O	174	*Numeric Coprocessor Reset* (386 mode) or *External Address Strobe* (486 mode). In 386 mode, this output resets the numeric coprocessor. This pin is asserted during CPU resets aand on I/O writes to I/O port F1h. Reset is synchronized with CLK2 and lasts for at least 40 clock cycles. In 486 mode, this output indicates an external device is driving a valid address and is used by the CPU for bus snooping/internal cache line invalidation.
NPINT	O	37	*Numeric Coprocessor Interrupt.* This output is generated when numeric coprocessor errors occur. It is connected to IRQ13 of interrupt controller.

3.4 LOCAL DRAM INTERFACE

Name	Type	Pin No.	Description
HIT#	I	4	***External Cache Hit.*** If this signal is active during a local memory read cycle, the memory controller will not respond and the external cache controller will complete the cycle. HIT# should be tied to VCC through a 10K pull-up resistor for non-cache systems.
DWE#	O	18	***DRAM Write Enable.*** This signal is typically buffered externally before being connected to the WE# input of the DRAMs.
RAS[3:0]#	O	22-19	***Row Address Strobes.*** Each RAS# signal corresponds to a unique DRAM bank. These signals are typically buffered externally before being connected to the RAS# input of the DRAMs.
CAS[7:0]#	O	32-25	***Column Address Strobes.*** The CAS[3:0]# outputs correspond to DRAM bank 0 and bank 2. The CAS[7:4]# outputs correspond to DRAM bank 1 and bank 3. These signals are typically connected directly to the DRAMs through a damping resistor.
MA[10:0]	O	7-17	***Memory Address bus.*** Multiplexed row/column address lines to the DRAM.
MP[3:0]	B	33-36	***Memory Parity bus.*** DRAM parity, one bit for each data byte.

3.5 BUS ARBITRATION

Name	Type	Pin No.	Description
HRQ	I	48	***Hold Request.*** DMA or MASTER cycle request from the 82C206.
HLDA	I	175	***Hold Acknowledge.*** This input is connected to the HLDA output from the CPU.
ADS8	I	44	***8-bit DMA transfer Address Strobe.*** The system controller uses this signal to latch XD[7:0] and pass them onto A[15:8].
AEN8#	I	45	***8-bit Address Enable.*** The system controller monitors this signal to decode 8-bit DMA cycles.
ADS16	I	42	***16-bit DMA transfer address strobe.*** The system controller uses this signal to latch XD(7:0) and pass them onto A(16:9).
AEN16#	I	43	***16-bit Address Enable.*** The system controller monitors this signal to decode 16-bit DMA cycles .
HOLD	O	172	***CPU Hold Request.*** This output is connected to the HOLD input of the CPU.
HLDA1	O	50	***Hold Acknowledge 1.*** This output indicates a hold acknowledge in response to a DMA or Master hold request. It is connected to the 82C206.
RFSH#	B	90	***Refresh.*** For normal CPU cycle, it is an output pin to indicate AT refresh cycles. It is an input pin for DMA or MASTER cycles. Note that the refresh cycle source is inside the chip and the refresh interval can be programmed to be either 16us (standard refresh) or 64 us (slow refresh).

3.6 AT-BUS INTERFACE

Name	Type	Pin No	Description
XA0	B	88	***System Address XA0.*** Input during master or 8-bit DMA cycles; output, otherwise.
XA1	B	89	***System Address XA1.*** Input during master and DMA cycles; output, otherwise.
CHRDY	I	87	***Channel Ready.*** This input, from the AT bus, uses a Schmitt trigger input pin.
0WS#	I	55	***Zero wait state.*** This input, from the AT bus, uses a Schmitt trigger input pin. System BIOS ROM cycles will be treated as zero wait state AT cycle.
IO16#	I	86	***16-bit IO slave.*** AT bus signal to indicate a 16-bit I/O slave is responding. It is a schmitt trigger input pin.
M16#	I	85	***16 bit memory slave.*** AT bus signal to indicate a 16-bit memory slave is responding. It is a schmitt trigger input pin.
GA20/A20M#	B	96	***Gated A20*** (386 mode) or ***A20 mask*** (486 mode). In 386 mode, it is the gated A20 (GA20) pin for the AT bus address line LA20. An external buffer is required between GA20 and LA20. It is normally an output, but becomes an input during Master cycles. In 486 mode, this is the mask A20 output to 486 .
IORD#	B	82	***AT IO read command.*** Normally an output, this pin becomes an input during master and DMA cycles.
IOWR#	B	81	***AT IO write command.*** Normally an output, this pin becomes an input during master and DMA cycles.
MRD#	B	80	***AT memory read command.*** Normally an output, this pin becomes an input during master and DMA cycles.
MWR#	B	79	***AT memory write command.*** Normally an output, this pin becomes an input during master and DMA cycles.
LMGCS#	O	57	***Low Megabyte Chip Select.*** Active when the memory area below 1Mbyte is accessed. It is used to qualify SMEMR# and SMEMW#. It is also active during refresh cycles.
ALE	O	84	***Address Latch Enable.*** ALE indicates the start of an AT cycle and is externally buffered before being connected to the AT bus. It is high during non-CPU cycles.
SBHE#	B	83	***System Byte High Enable.*** AT bus byte high enable. Normally an output, this pin becomes an input during master cycles.
INTA#	O	49	***Interrupt Acknowledge.*** The system controller drives this signal to acknowledge an interrupt cycle.
ROMOE#	O	52	***System BIOS ROM Output Enable.*** The system BIOS can be accessed as either an 8-bit or a 16-bit device based on the M16# input. For CPU accesses, ROMOE# is active from the end of the first T2 until 1/2 of a T-state after the last T2. For non-CPU accesses, ROMOE# is active along with MEMRD#.
XD(15:0)	B	78-71, 68-61	***System data bus.*** This is typically used as the databus for on-board peripherals. A buffer is required between this bus (XD) and the AT data bus (SD). SDIR1, SDIR2 and SDEN# control this buffer logic.
SDIR1	O	59	***SD bus Low Byte Direction Control.*** This signal controls the direction of the low byte buffer between the XD (XD[7:0]) and the SD bus. A high on this signal points the buffer from the XD bus to the SD bus.

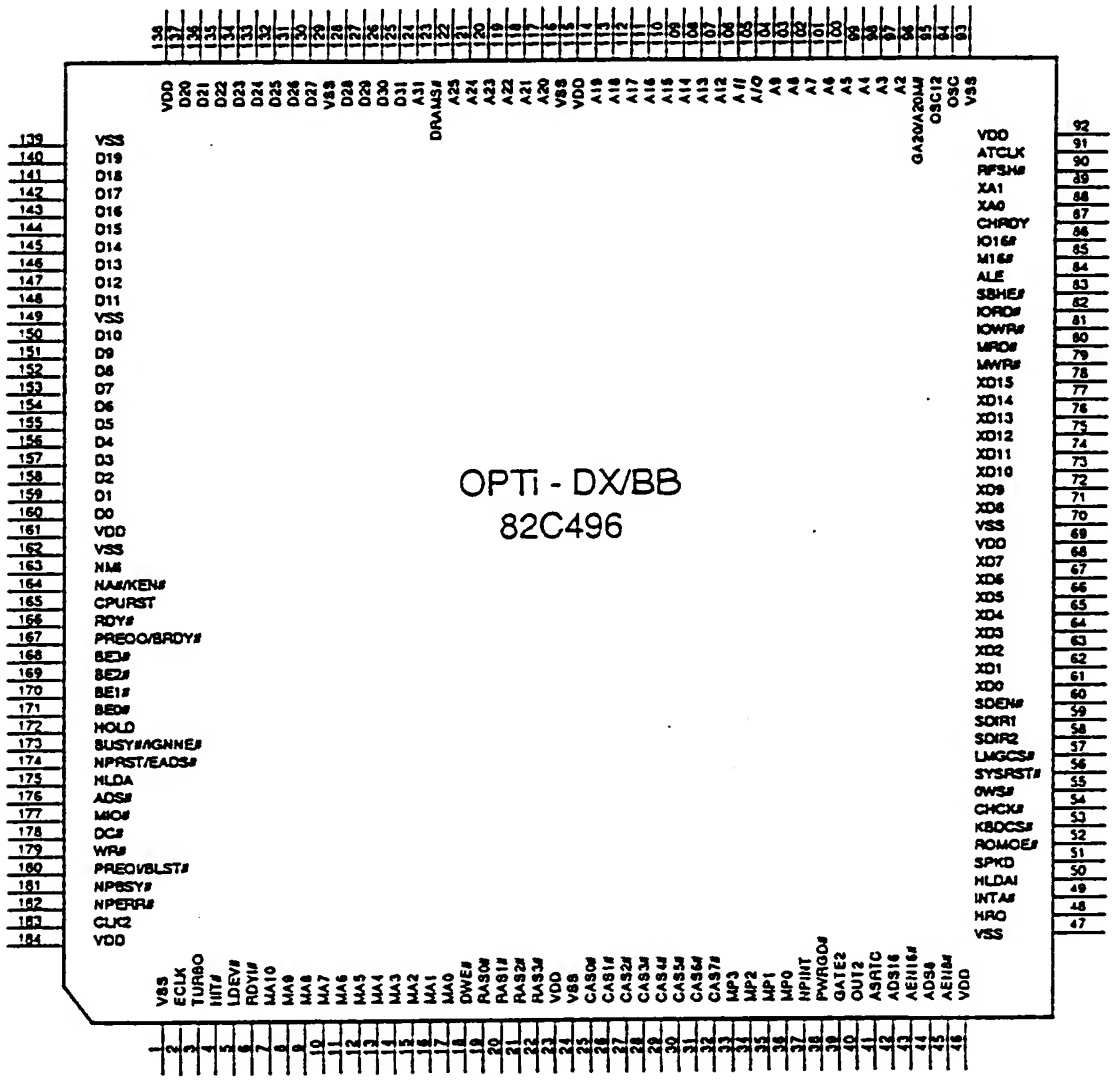
SDIR2	O	58	***SD bus High Byte Direction Control.*** This signal controls the direction of the high byte buffer between the XD (XD[15:8]) and the SD bus. A high on this signal points the buffer from the XD bus to the SD bus.
SDEN#	O	60	***AT Data bus Buffer Enable.*** This signal controls the output enable of the SD/XD buffers. It is enabled for CPU accesses to the AT bus.
CHCK#	I	54	***AT bus Channel Check.*** This signal, from the AT bus, is used as one of the sources to generate a CPU NMI.

3.7 MISCELLANEOUS SIGNALS

Name	Type	Pin No.	Description
KBDCS#	O	53	***Keyboard Controller chip select.*** The system controller decodes accesses to the keyboard controller and, when appropriate, issues this chip select signal.
NMI	O	163	***Non-maskable interrupt.*** It is activated when either a parity error from local memory read is detected or when the CHCK# signal from AT bus is asserted (and their corresponding control bit in Port B is also enabled).
GATE2	O	39	***Timer 2 gate control.*** This signal is used as the gate 2 input in the 8254 compatible timer logic of the integrated peripheral controller (82C206).
SPKD	O	51	***Speaker Data.*** SPKD is a function of OUT2 and port 61h<1>.
ASRTC	O	41	***Real Time Clock (RTC) address strobe.***
OUT2	I	40	***Timer 2 output.*** This signal, from the timer 2 output of the 8254 compatible circuit in the 82C206, is used as an input for the speaker data logic.

3.8 GROUND & VCC

Name	Type	Pin No	Description
VCC	I	23,46,69,92,115,138,161,184	+5V
GND	I	1,24,47,70,93,116,129,139,149,162	VSS or Ground


OPTi - DX/BB
82C496
VSS
D19
D18
D17
D16
D15
D14
D13
D12
D11
VSS
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
VDD
VSS
NMI
NA#/KEN#
CPURST
RDY#
PREQO/BRDY#
BE3#
BE2#
BE1#
BE0#
HOLD
BUSY#/GNNE#
NPRST/EADS#
HLDA
ADS#
M/IO#
D/C#
W/R#
PREQI/BLST#
NPBSY#
NPERR#
CLK2
VDD
VDD
ATCLK
RFSH#
XA1
XA0
CHRDY
IO16#
M16#
ALE
SBHE#
IORD#
IOWR#
MRD#
MWR#
XD15
XD14
XD13
XD12
XD11
XD10
XD9
XD8
VSS
VDD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
SDEN#
SDIR1
SDIR2
LMGCS#
SYSRST#
0WS#
CHCK#
KBDCS#
ROMCE#
SPKD
HLDAI
INT#
HRQ
VSS
VSS
ECLK
TURBO
IIIT#
LDEV#
RDY#
MA10
MA9
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
DWE#
RASO#
RAS1#
RAS2#
RAS3#
VDD
VSS
CAS0#
CAS1#
CAS2#
CAS3#
CAS4#
CAS5#
CAS6#
CAS7#
MP3
MP2
MP1
MP0
NPINT
PWRGD#
GATE2
OUT2
ASRTC
ADS16
AEN16#
ADS#
AEN1#
VDD
VDD
D20
D21
D22
D23
D24
D25
D26
D27
VSS
D28
D29
D30
D31
A31
DRAM3#
A25
A24
A23
A22
A21
A20
VSS
VDD
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
GA20/A20M#
OSC12
OSC
VSS

82C496 Numerical Pin Cross Reference

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	47	VSS	93	VSS	139	VSS
2	ECLK	48	HRQ	94	OSC	140	D19
3	TURBO	49	INTA#	95	OSC12	141	D18
4	HIT#	50	HLDA1	96	GA20/A20M#	142	D17
5	LDEV#	51	SPKD	97	A2	143	D16
6	RDYI#	52	ROMOE#	98	A3	144	D15
7	MA10	53	KBDCS#	99	A4	145	D14
8	MA9	54	CHCK#	100	A5	146	D13
9	MA8	55	0WS#	101	A6	147	D12
10	MA7	56	SYSRST#	102	A7	148	D11
11	MA6	57	LMGCS#	103	A8	149	VSS
12	MA5	58	SDIR2	104	A9	150	D10
13	MA4	59	SDIR1	105	A10	151	D9
14	MA3	60	SDEN#	106	A11	152	D8
15	MA2	61	XD0	107	A12	153	D7
16	MA1	62	XD1	108	A13	154	D6
17	MA0	63	XD2	109	A14	155	D5
18	DWE#	64	XD3	110	A15	156	D4
19	RAS0#	65	XD4	111	A16	157	D3
20	RAS1#	66	XD5	112	A17	158	D2
21	RAS2#	67	XD6	113	A18	159	D1
22	RAS3#	68	XD7	114	A19	160	D0
23	VDD	69	VDD	115	VDD	161	VDD
24	VSS	70	VSS	116	VSS	162	VSS
25	CAS0#	71	XD8	117	A20	163	NMI
26	CAS1#	72	XD9	118	A21	164	NA#/KEN#
27	CAS2#	73	XD10	119	A22	165	CPURST
28	CAS3#	74	XD11	120	A23	166	RDY#
29	CAS4#	75	XD12	121	A24	167	PREQO/BRDY#
30	CAS5#	76	XD13	122	A25	168	BE3#
31	CAS6#	77	XD14	123	DRAMS#	169	BE2#
32	CAS7#	78	XD15	124	A31	170	BE1#
33	MP3	79	MWR#	125	D31	171	BE0#
34	MP2	80	MRD#	126	D30	172	HOLD
35	MP1	81	IOWR#	127	D29	173	BUSY#/IGNNE#
36	MP0	82	IORD#	128	D28	174	NPRST/EADS#
37	NPINT	83	SBHE#	129	VSS	175	HLDA
38	PWRGD#	84	ALE	130	D27	176	ADS#
39	GATE2	85	M16#	131	D26	177	M/IO#
40	OUT2	86	IO16#	132	D25	178	D/C#
41	ASRTC	87	CHRDY	133	D24	179	W/R#
42	ADS16	88	XA0	134	D23	180	PREQI/BLST#
43	AEN16#	89	XA1	135	D22	181	NPBSY#
44	ADS8	90	RFSH#	136	D21	182	NPERR#
45	AEN8#	91	ATCLK	137	D20	183	CLK2
46	VDD	92	VDD	138	VDD	184	VDD

4.0 82C496 AC/DC SPECIFICATIONS

82C496-20/25/33/40 Mhz DC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Symbol	Description	Min	Max	Units
VIL	Input low voltage	-0.3	0.8	V
VIH	Input high voltage	2.0	Vcc+0.3	V
VOL	Ouput low voltage IOL = 3.0 MA all pins except IOL = 6.0 MA for Group A IOL = 12.0 MA for Group B		0.45	V
VOH	Output high voltage IOH = -1.6 MA all pins except IOH = -3.2 MA for Group A IOH = -6.4 MA for Group B	2.4		V
IIL	Input leakage current, VIN=Vcc 0V < VIN < Vcc	-10	10	uA
IOZ	Tristate leakage current 0.45V < VOUT < Vcc		10	uA
CIN	Input capacitance		20	pF
COUT	Output capacitance		20	pF
CIO	I/O Capacitance		20	pF
ICC	Power supply current @ 33MHz		50	MA

Group A pins : LD(0:15), MP (0:1), RDYO#, ATCLK, MA(0:9), RAS(0:3)#, CAS(0:7)#

Group B pins : GA20/A20M#, PCLK2,SD(0:15), MEMRD#, RFSH#, M16#

82C496 Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VCC	Supply voltage	-0.5	6.5	V
VI	Input voltage	-0.5	VCC+0.5	V
VO	Output voltage	-0.5	VCC+0.5	V
TOP	Operating Temperature	0	70	C
TSTG	Storage temperature	-40	125	C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

82C496/82C496-33 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Sym	Description	Min	Typ	Max	Units
t101	ECLK raising edge to CLK2 raising delay	3		8	ns
t102	ECLK falling edge to CLK2 raising delay	3		8	ns
t103	LDEV# to CLK2 raising edge setup time	5			ns
t104	LDEV# to CLK2 raising edge hold time	3			ns
t105	ADS# to CLK2 raising edge setup time	5			ns
t106	ADS# to CLK2 raising edge hold time	3			ns
t107	ADDR to CLK2 raising edge setup time	5			ns
t108	ADDR to CLK2 raising edge hold time	3			ns
t111	READY# to CLK2 setup time	9			ns
t112	READY# to CLK2 hold time	6			ns
t113	CLK2 to CPURST/NPRST active delay		10		ns
t114	CLK2 to CPURST/NPRST inactive delay		10		ns
t117	NPBSY# active width	13			ns
t118	NPERR# to NPBUSY# hold time	5			ns
t119	NPERR# to NPBUSY# setup time	5			ns
t120	NPBUSY# active to BUSY# active delay	8	12		ns
t121	NPBUSY# inactive to BUSY# inactive dly	8	12		ns
t122	NPERR# low pulse width	8			ns
t123	IOW# active to BUSY# inactive delay		12		ns
t124	IOW# active width (for NP reset cycle)		256 x	CLK2	
t125	NPRST active width (to 0F1)		40 x	CLK2	

82C496/82C496-33 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

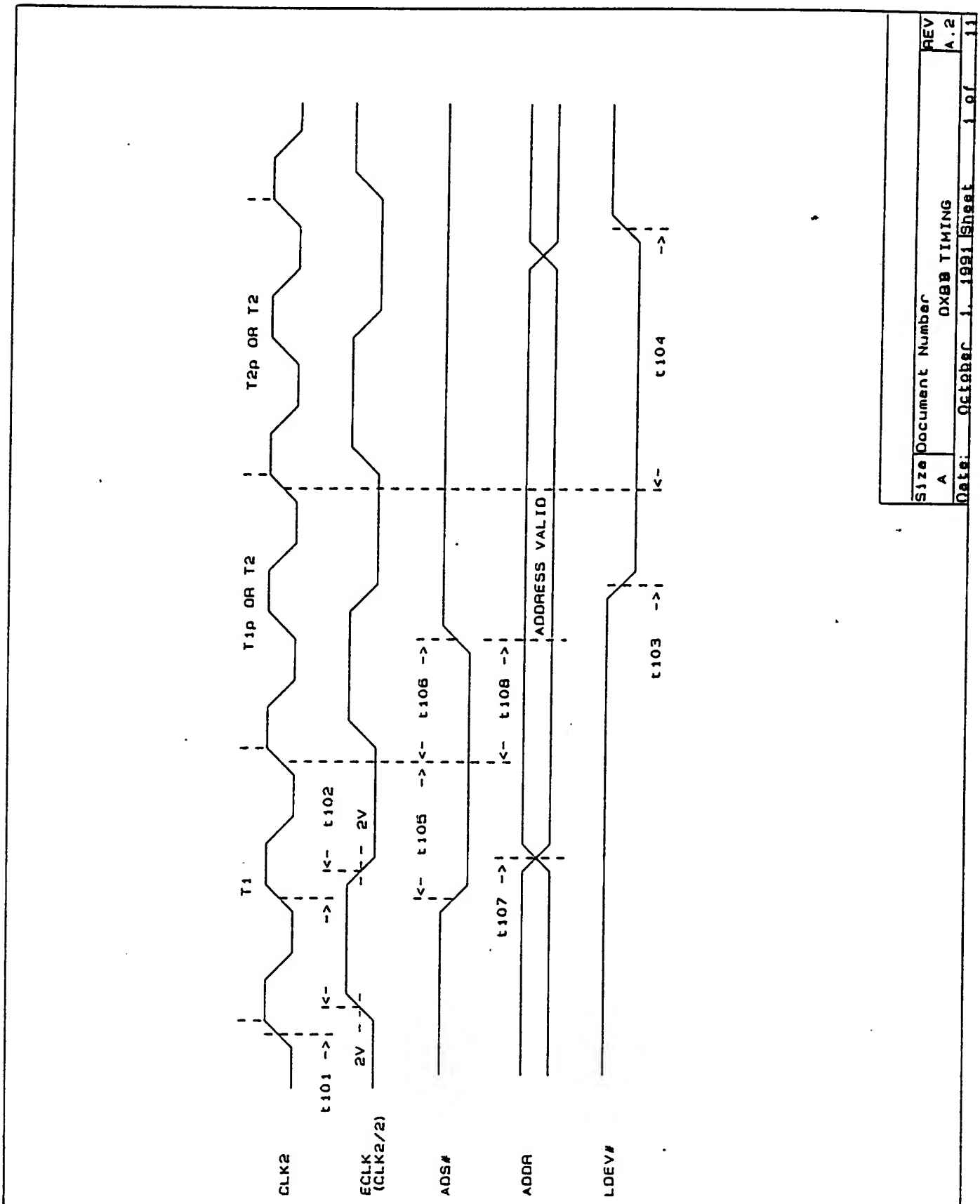
Sym	Description	Min	Typ	Max	Units
t202	CLK2 to CAS# active delay	10		16	ns
t203	CLK2 to CAS# inactive delay	11		18	ns
t204	CLK2 to RDY# active delay	10	15	19	ns
t205	CLK2 to RDY# inactive delay	10	15	19	ns
t206	CLK2 to RAS# inactive delay	10	15	19	ns
t207	CLK2 to RAS# active delay	8		16	ns
t208	Non CPU cycle CMD to RAS# active delay		2		CLK2
t209	Non CPU cycle CMD inactive to RAS# inact. delay		2		CLK2
t210	Non CPU cycle RAS active to CAS# address valid		2		CLK2
t211	Non CPU cycle RAS active to CAS# active delay		4		CLK2
t212	Non CPU cycle CMD inactive to CAS# inactive delay		2		CLK2
t213	Non CPU cycle CMD active to DWE# active delay		2		CLK2
t214	Non CPU cycle CMD inactive to DWE# inactive delay		2		CLK2
t215	REF# active to CAS0-3# active delay		4		CLK2
t216	CAS0-3# active to CAS4-7# active delay		1		CLK2
t217	CAS4-7# active to RAS0,2# active delay		1		CLK2
t218	RAS1,3# active to RAS0,2# active delay		1		CLK2
t219	CLK2 to DWE# active delay	8		16	ns
t220	CLK2 to DWE# inactive delay	4		10	ns
t221	CLK2 to MA0-9 valid delay	8		16	ns
t222	CLK2 to MA0-9 change delay	8		16	ns
t223	REF# active period		4		ATcyc
t224	On board DRAM refresh period		9		CLK2
t225	MA0-9 to RAS# hold time		2		CLK2
t226	MA0-9 to CAS# setup time		2		CLK2
t227	RAS# precharge time		4		CLK2

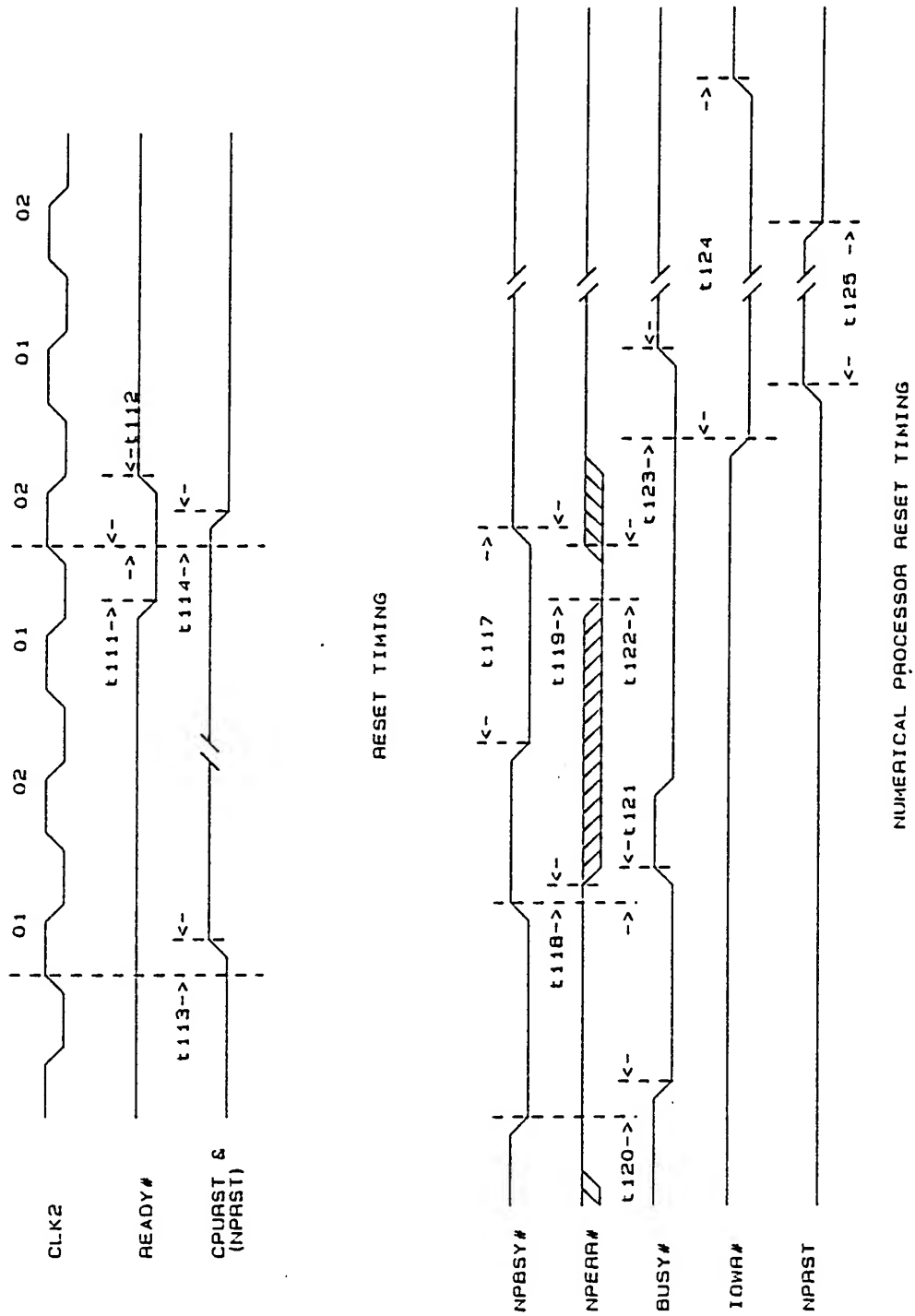
82C496/82C496-33 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

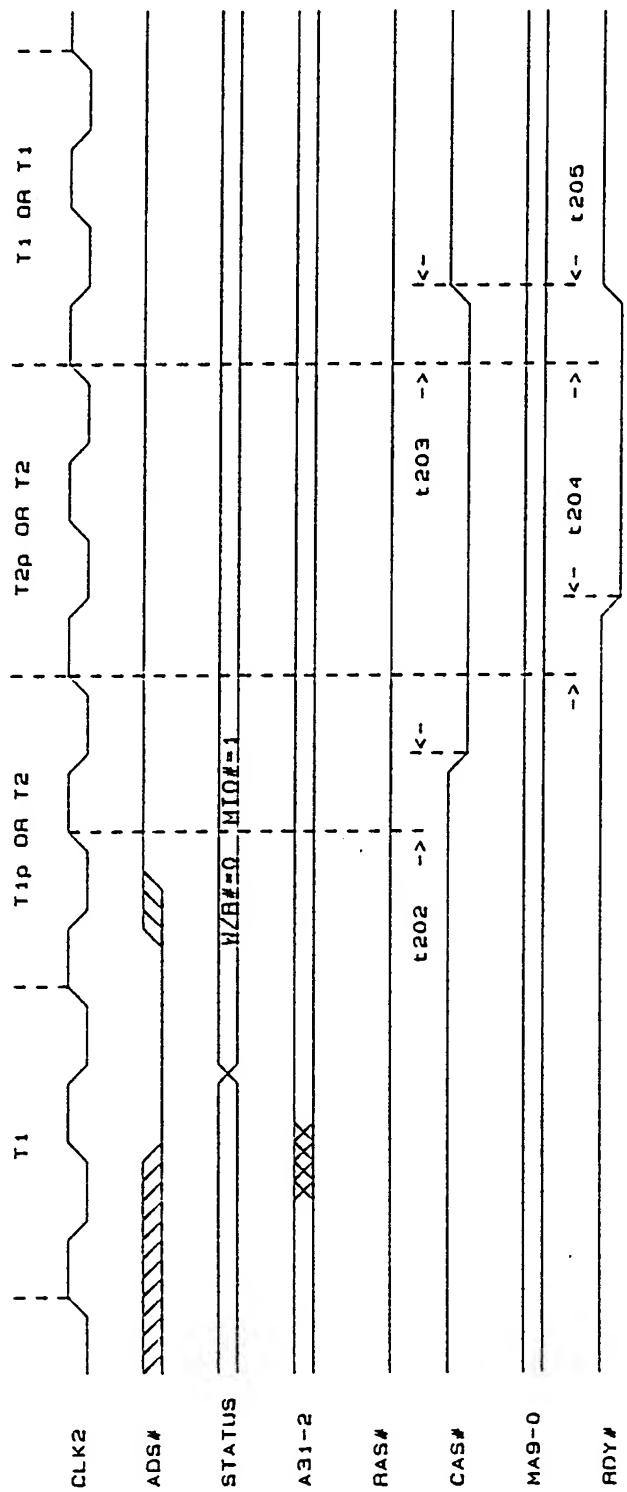
Sym	Description	Min	Typ	Max	Units
t301	D(31:0) active to XD(15:0) delay	9		17	ns
t302	D(31:0) active to MP(3:0) delay	8		18	ns
t303	D(31:0) inactive to XD(15:0) delay	8		18	ns
t304	D(31:0) inactive to MP(3:0) delay	8		18	ns
t305	XD(15:0) active to D(31:0) delay	8		16	ns
t306	XD(15:0) active to PM(3:0) delay	12		20	ns
t307	XD(15:0) inactive to D(31:0) delay	8		16	ns
t308	XD(15:0) inactive to MP(3:0) delay	12		20	ns
t309	XD(15:0) to IOR#,MRD# setup time	5			ns
t310	XD(15:0) to IOR#,MRD# hold time	5			ns
t311	XD(15:8) active to XD(7:0) delay	8		16	ns
t312	XD(15:8) inactive to XD(7:0) delay	9		18	ns
t313	CHCK# active to NMI delay		18		ns
t314	IOWR# inactive to GATE2, NMI, SPKDATA change		20		ns
t315	XA(9:0) to KBDCS# active delay	10	14		ns
t316	XA(9:0) to KBDCS# inactive delay	10	14		ns

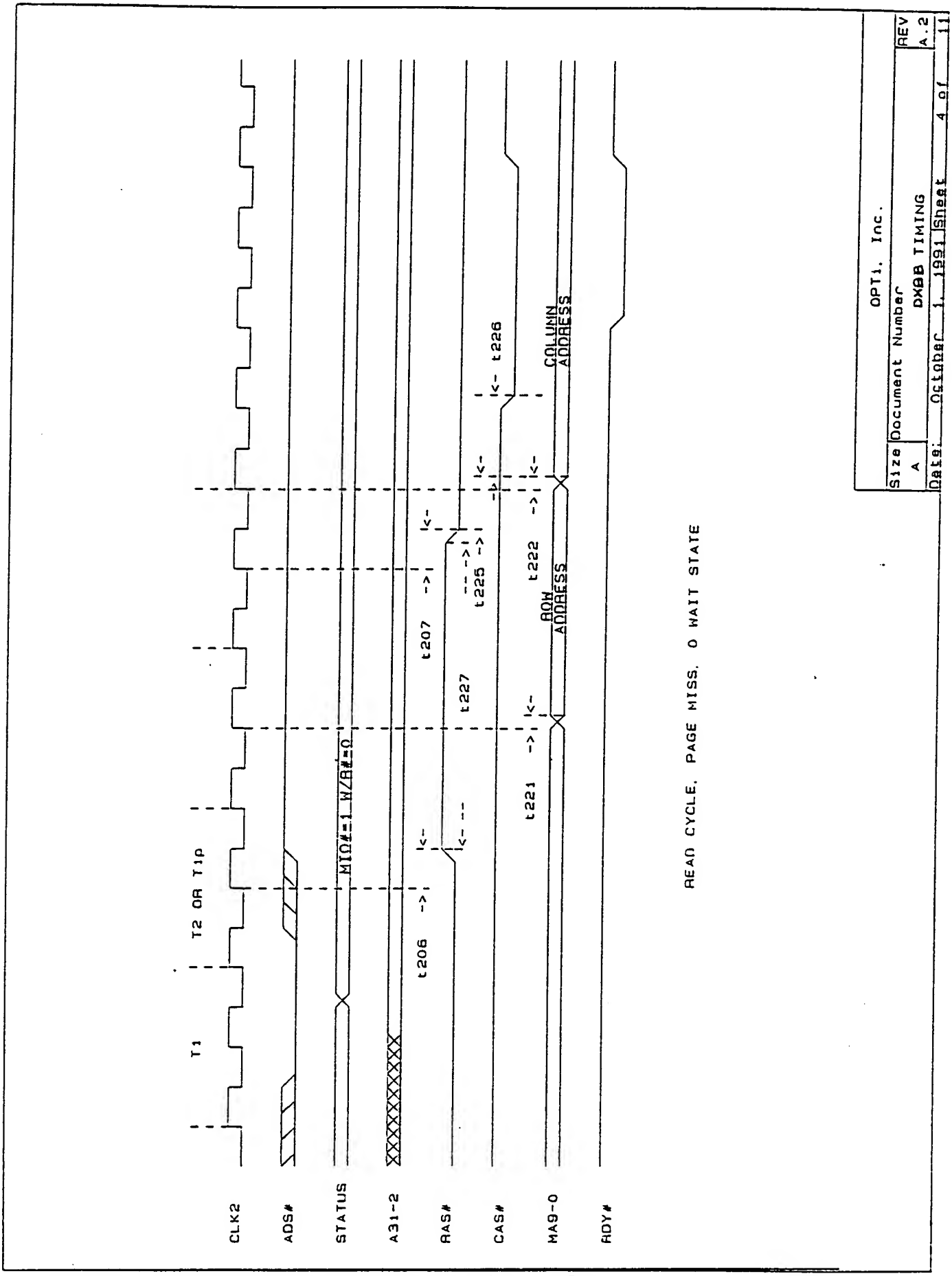
82C496/82C496-33 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

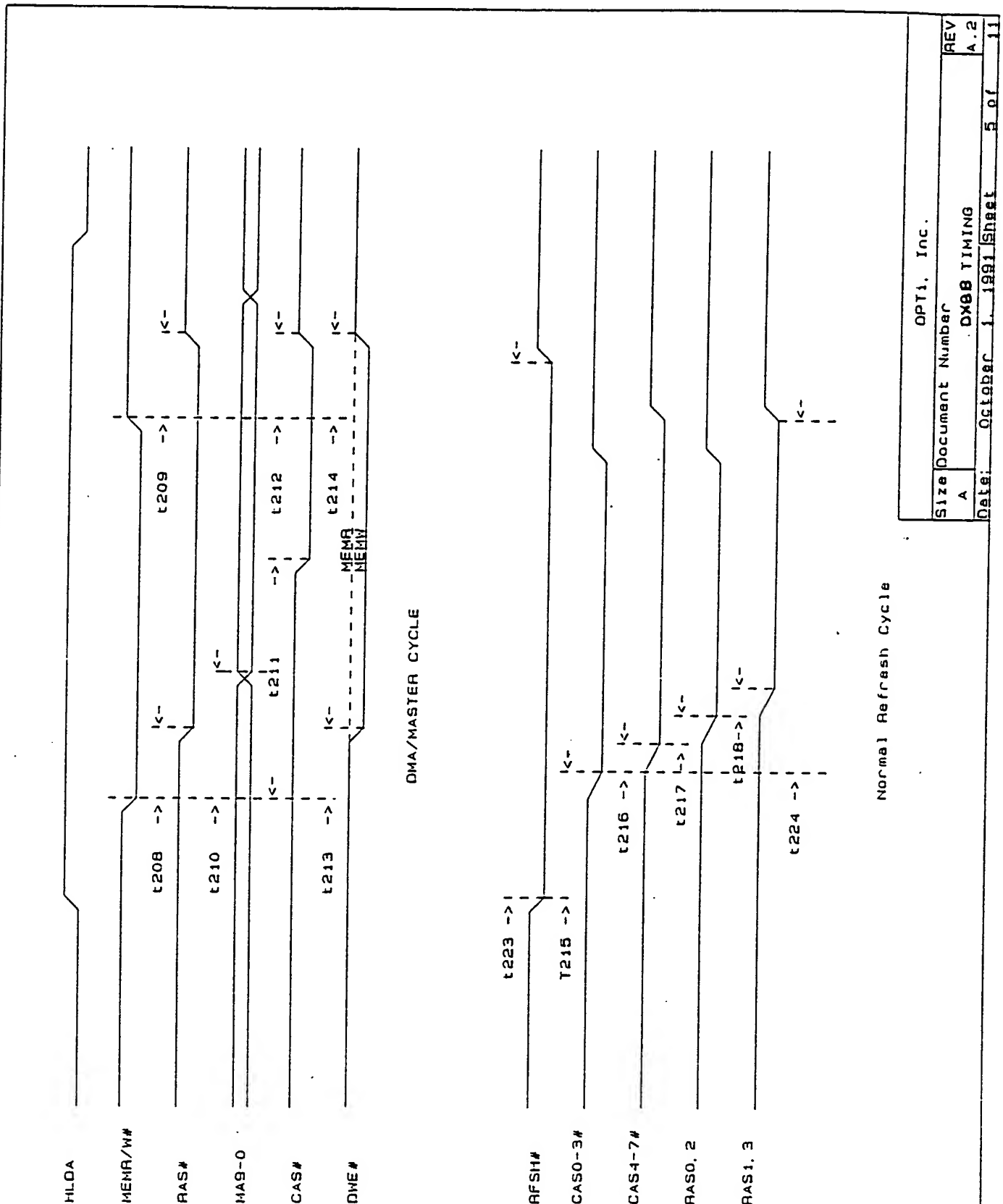
Sym	Description	Min	Typ	Max	Units
t501	ATCLK falling to ALE active delay		1	2	ns
t502	ATCLK to ALE inactive delay		.8	1.2	ns
t503	ATCLK falling to CMD active delay		2	4	ns
t503.1	ATCLK falling to 16 bit CMD active delay		2	4	ns
t504	ATCLK to CMD inactive delay		2	4	ns
t505	M16# to ATCLK setup time	8			ns
t506	M16# to ATCLK hold time	4			ns
t507	IO16# to ATCLK setup time	10			ns
t508	IO16# to ATCLK hold time	10			ns
t509	0WS# to ATCLK setup time	9			ns
t510	0WS# to ATCLK hold time	4			ns
t511	CHRDY to ATCLK setup time	11			ns
t512	CHRDY to ATCLK hold time	4			ns
t513	CLK2 to HOLD active delay	6	10		ns
t514	CLK2 to HOLD inactive delay	5	9		ns
t516	ATCLK toREF# inactive delay	20	30		ns
t517	ATCLK to MRD# active delay	3	5		ns
t518	ATCLK to MRD# inactive delay	8	15		ns
t519	HRQ to ATCLK setup time	10			ns
t520	HRQ to ATCLK hold time	4			ns
t521	HLDA to HLDA1 active delay	8		17	ns
t522	HLDA to HLDA1 inactive delay	12		18	ns
t523	CLK2 to SDIR1,2 active delay		12	15	ns
t524	CLK2 to SDIR1,2 inactive delay		13	15	ns
t525	CLK2 to SDEN active delay		15	25	ns
t526	CLK2 to SDEN inactive delay		16	25	ns
t527	NPBUSY# to NPERR# setup time	3			ns
t528	NPERR# active to NPINT active dealy			10	ns

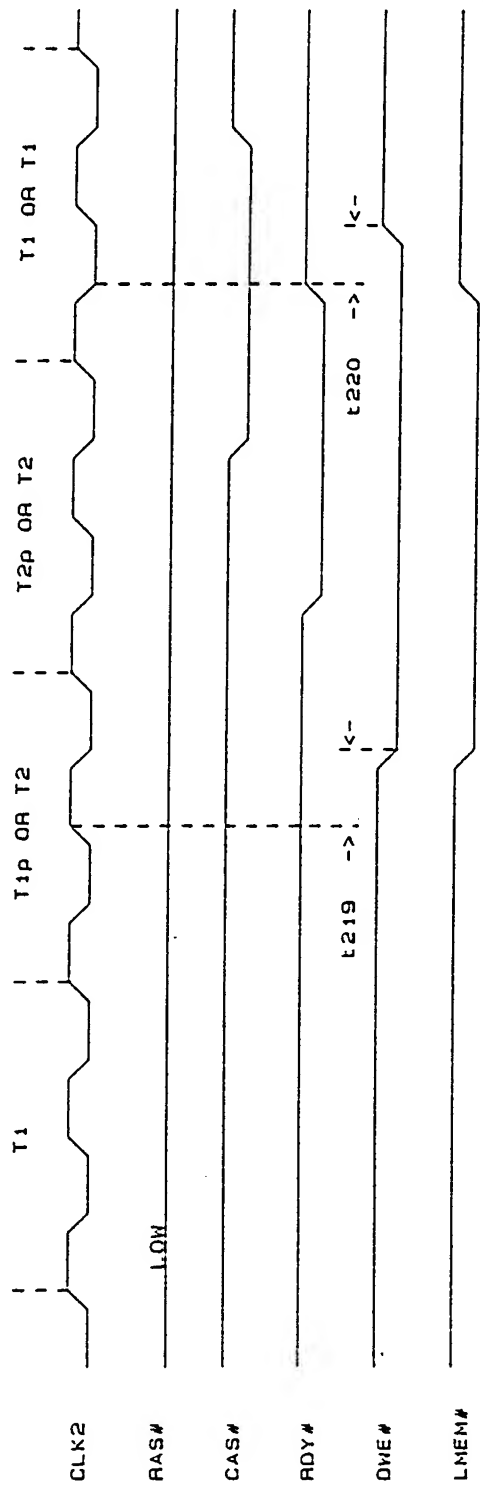

CLK2
ECLK (CLK2/2)
ADS#
ADDR
LDEV#
t101
t102
t103
t104
t105
t106
t107
t108
T1
T1p OR T2
T2p OR T2
2V
ADDRESS VALID
Size A
Document Number DXBB TIMING
REV A.2
Date: October 1, 1991 Sheet 1 of 11


RESET TIMING
CLK2
READY#
CPURST & (NPRST)
NPBSY#
NPERR#
BUSY#
IOWR#
NPRST
t111
t112
t113
t114
t117
t118
t119
t120
t121
t122
t123
t124
t125
01
02
NUMERICAL PROCESSOR RESET TIMING
OPTi Inc.
Size A
Document Number ATBUS 3
REV A.2
Date: October 1, 1991 Sheet 2 of 11


T1
T1p OR T2
T2p OR T2
T1 OR T1
CLK2
ADS#
STATUS
A31-2
RAS#
CAS#
MA9-0
RDY#
W/R#=0
M/IO#=1
t202
t203
t204
t205
386 READ CYCLE, PAGE HIT, 0 WAIT STATE
486 READ CYCLE, PAGE HIT, 0 WS BURST MODE
3-2-2-2
Opti, Inc.
Size
A
Document Number
DXBB TIMING
REV
A.2
Date: October 1, 1991 Sheet 3 of 11


T1
T2 OR T1P
CLK2
ADS#
STATUS
A31-2
RAS#
CAS#
MA9-0
RDY#
M/IO#=1 W/R#=0
t206
t207
t227
t225
t221
t222
t226
ROW ADDRESS
COLUMN ADDRESS
READ CYCLE, PAGE MISS, 0 WAIT STATE
OPTi, Inc.
Size A
Document Number DXBB TIMING
REV A.2
Date: October 1, 1991 Sheet 4 of 11


HLDA
MEMR/W#
RAS#
MA9-0
CAS#
DWE#
t208
t209
t210
t211
t212
t213
t214
MEMR
MEMW
DMA/MASTER CYCLE
RFSH#
CAS0-3#
CAS4-7#
RAS0, 2
RAS1, 3
t223
T215
t216
t217
t218
t224
Normal Refresh Cycle
OPTi, Inc.
Size
A
Document Number
DXBB TIMING
REV
A.2
Date: October 1, 1991 Sheet 5 of 11

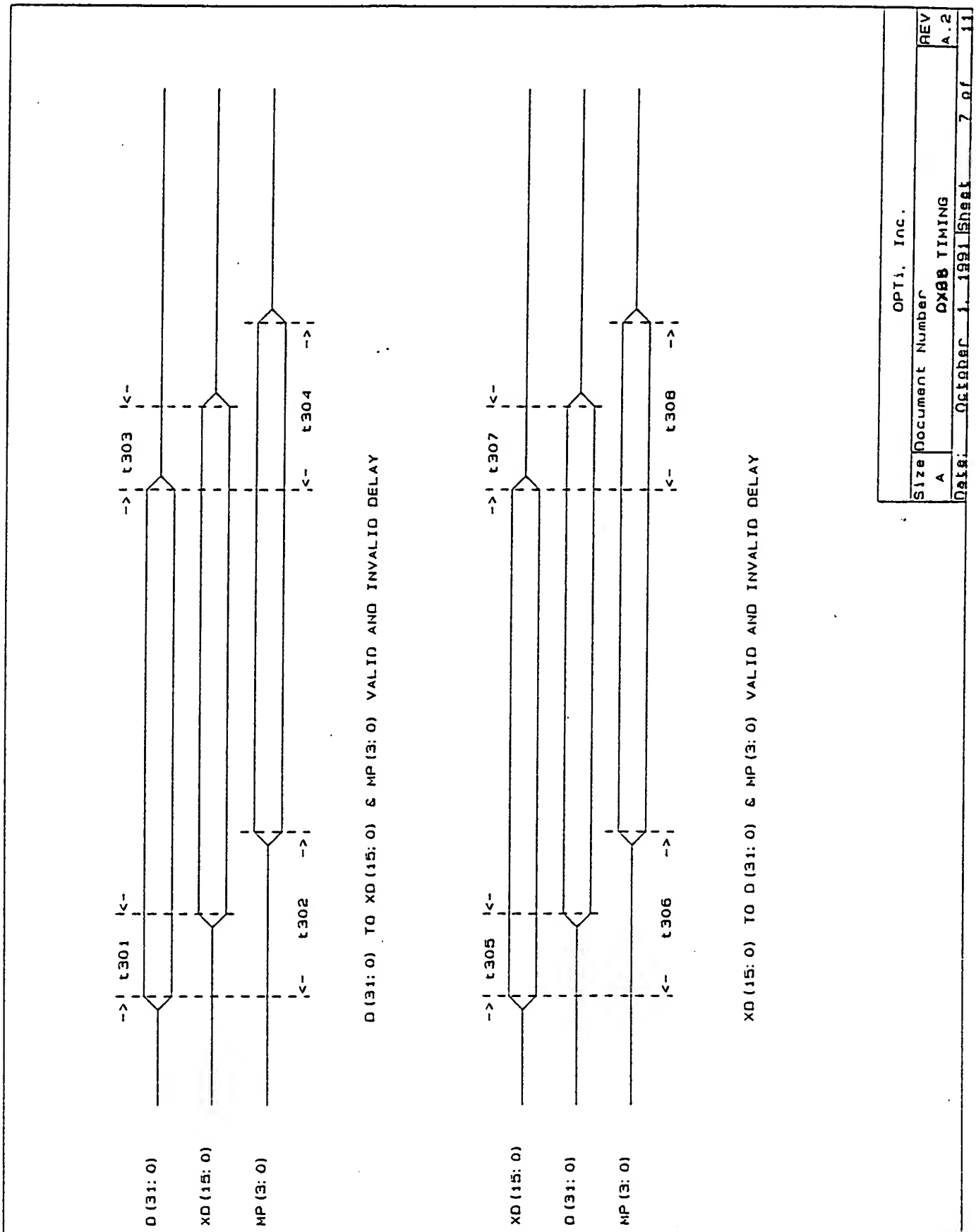


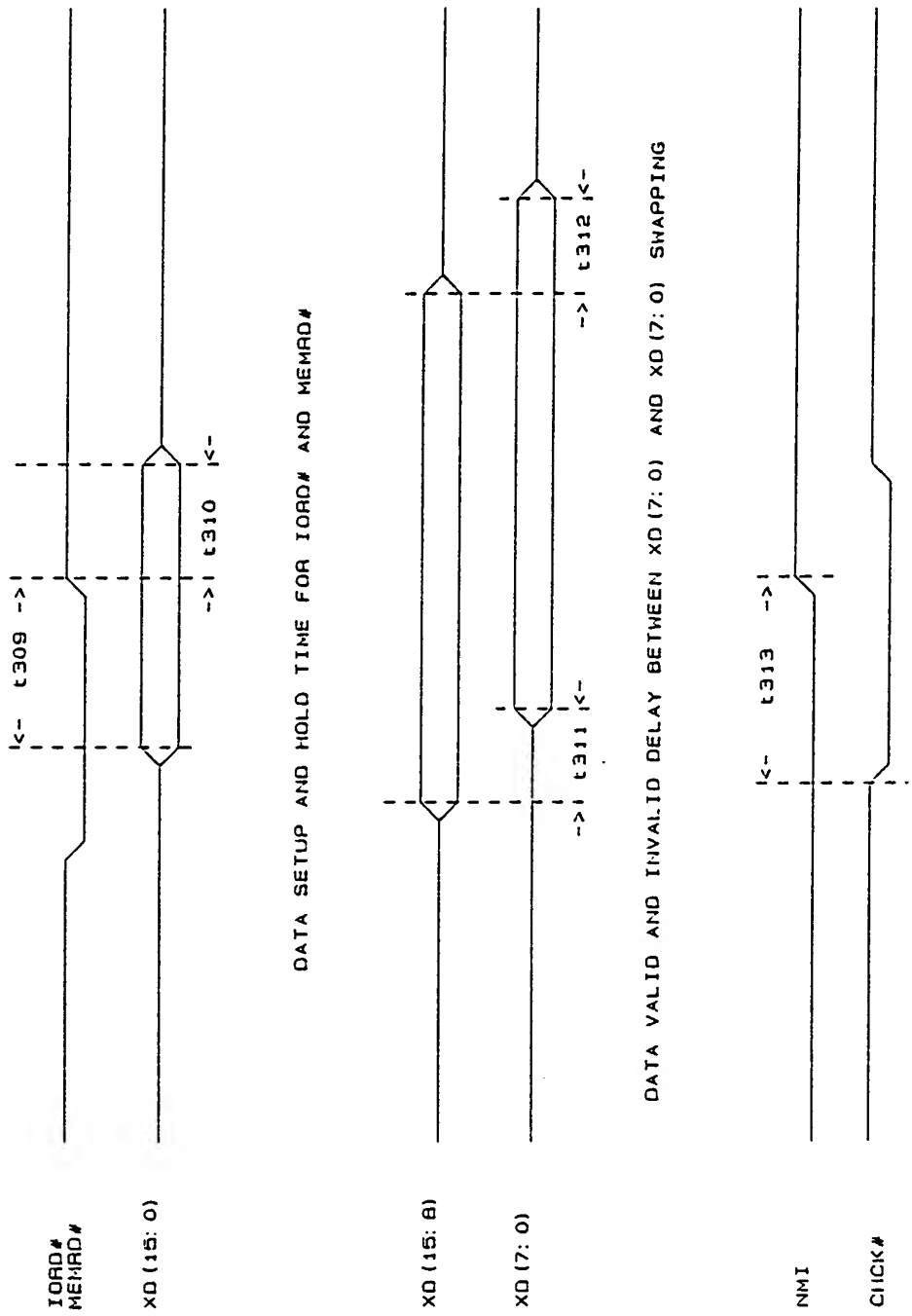
WRITE CYCLE, PAGE HIT, 0 WAIT STATE

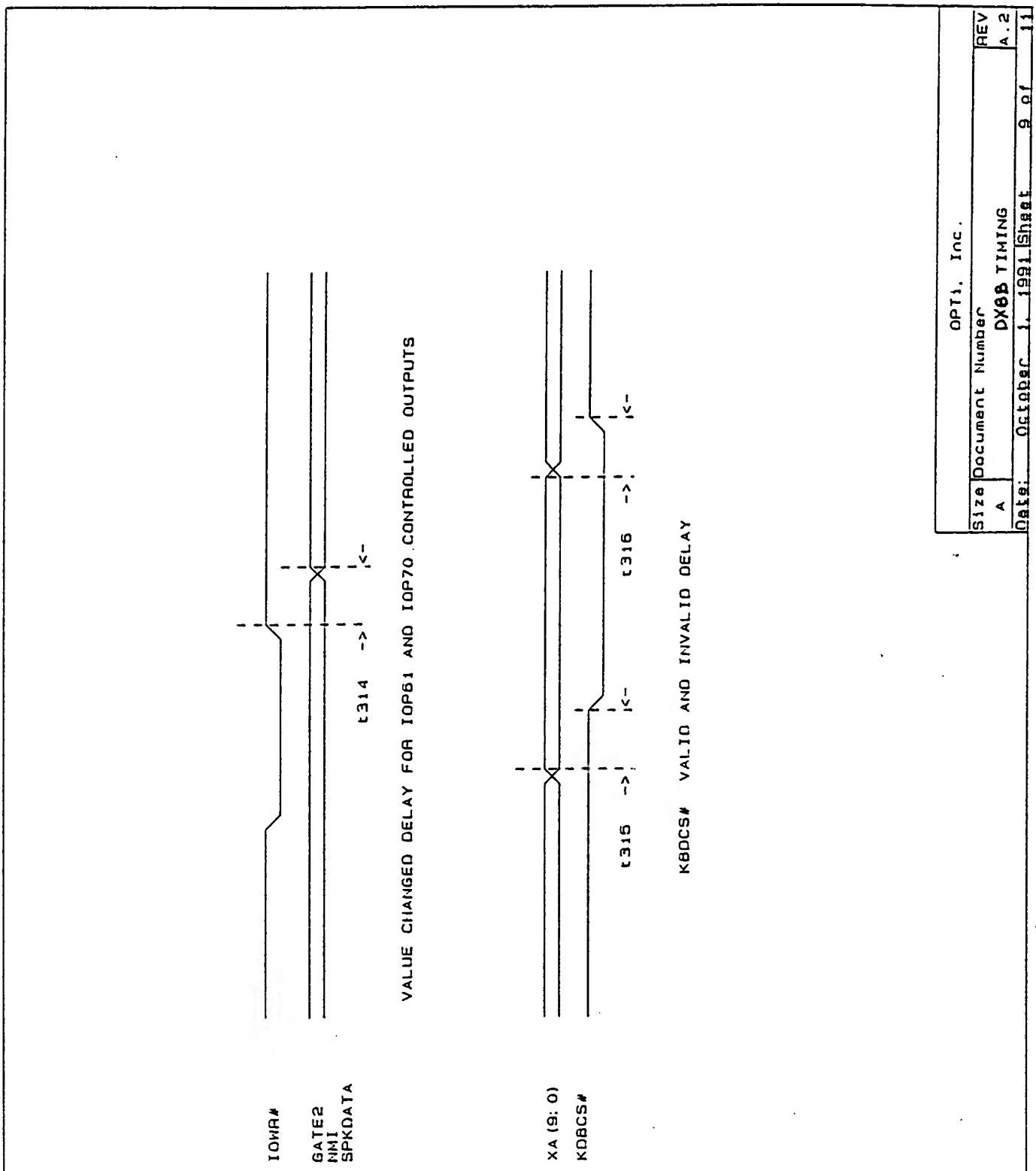
Opti, Inc.

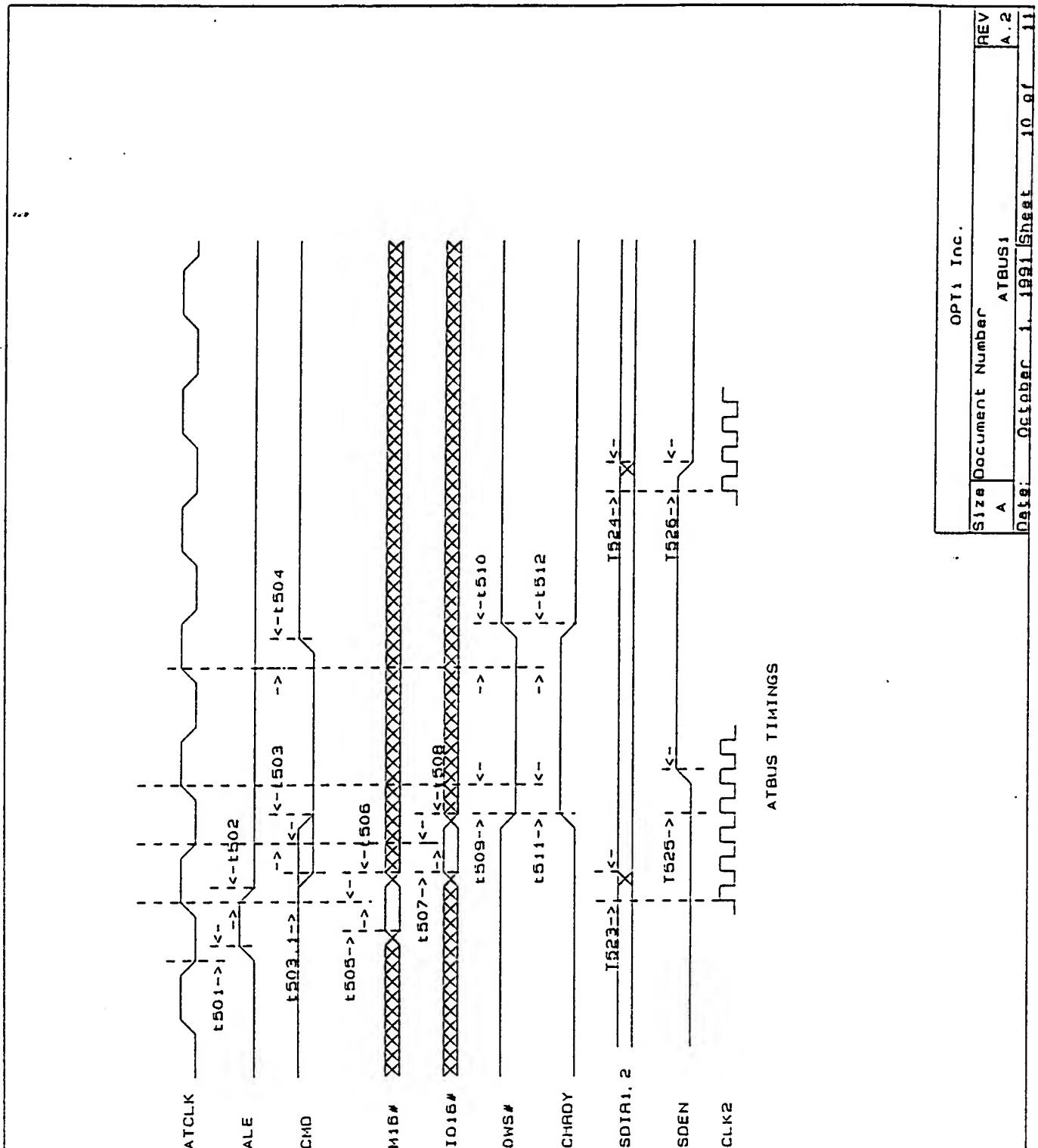
Size	Document Number	REV
A	DXBB TIMING	A.2

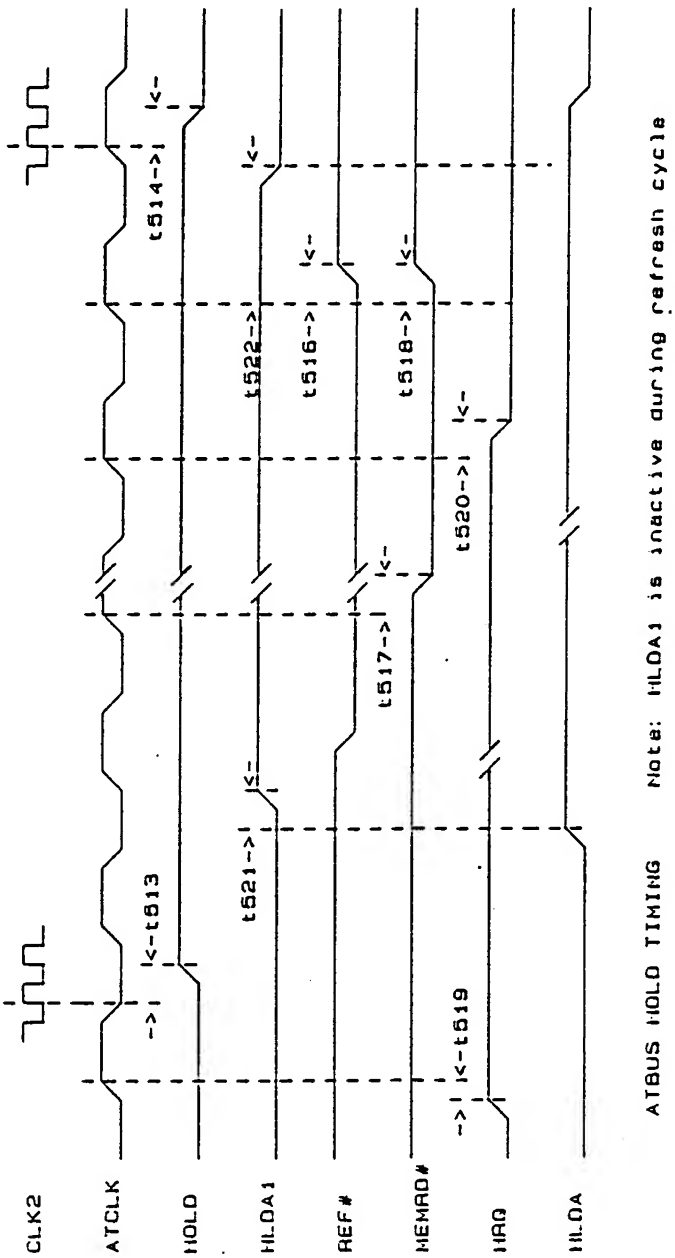
Date: October 1, 1991 Sheet 6 of 11

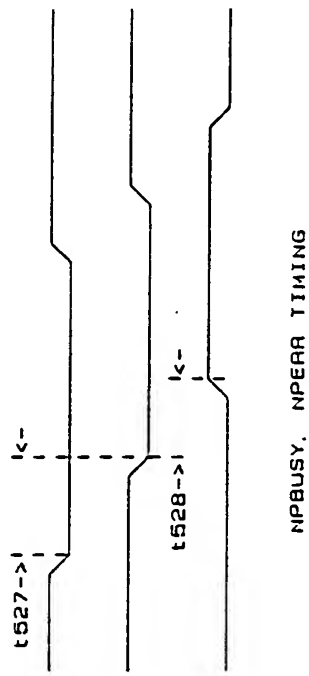

OPTi, Inc.
Size
A
Document Number
DX8B TIMING
REV
A.2
Date: October 1, 1991 Sheet 7 of 11
D(31:0)
XD(15:0)
MP(3:0)
t301
t302
t303
t304
D(31:0) TO XD(15:0) & MP(3:0) VALID AND INVALID DELAY
XD(15:0)
D(31:0)
MP(3:0)
t305
t306
t307
t308
XD(15:0) TO D(31:0) & MP(3:0) VALID AND INVALID DELAY

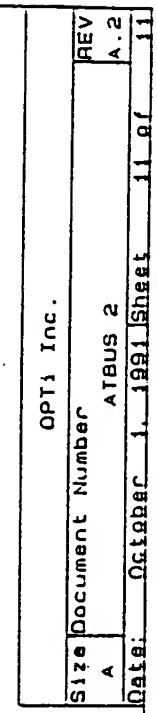

IORD#
MEMRD#
XD(15:0)
t309
t310
DATA SETUP AND HOLD TIME FOR IORD# AND MEMRD#
XD(15:8)
XD(7:0)
t311
t312
DATA VALID AND INVALID DELAY BETWEEN XD(7:0) AND XD(7:0) SWAPPING
NMI
CLICK#
t313
NMI VALID DELAY RELATED TO CHCK#
OPTi, Inc.
Size
A
Document Number
DX8B TIMING
REV
A.2
Date: October 1, 1991 Sheet 8 of 11

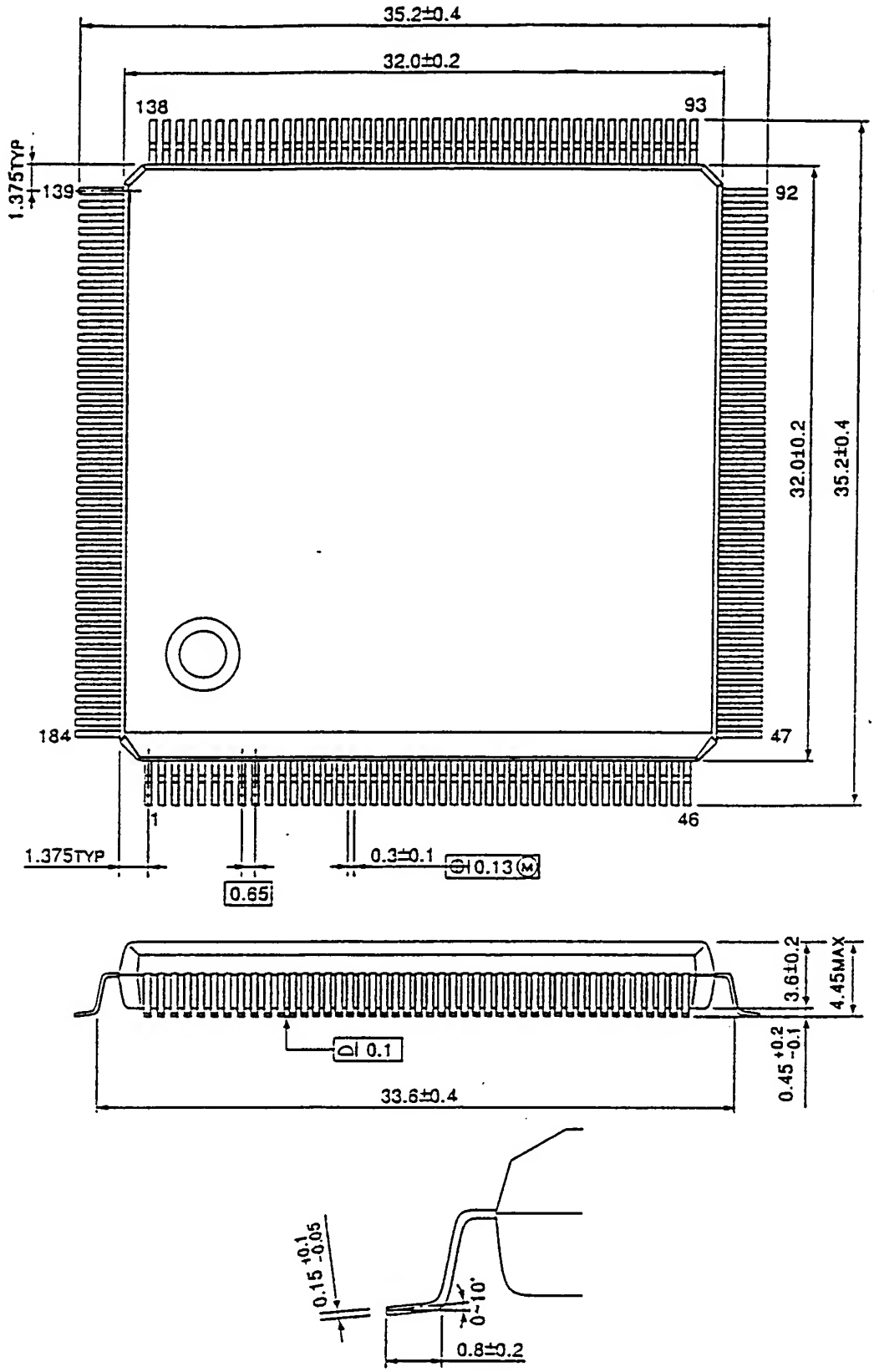

IOWR#
GATE2
NMI
SPKDATA
t314
VALUE CHANGED DELAY FOR IOP61 AND IOP70 CONTROLLED OUTPUTS
XA(9:0)
KBDCS#
t315
t316
KBDCS# VALID AND INVALID DELAY
OPTi, Inc.
Size A
Document Number DXBB TIMING
REV A.2
Date: October 1, 1991 Sheet 9 of 11


ATCLK
ALE
CMD
M16#
IO16#
OWS#
CHRDY
SDIR1, 2
SDEN
CLK2
t501->
t502
t503
t503.1->
t504
t505->
t506
t507->
t508
t509->
t510
t511->
t512
I523->
I524->
I525->
I526->
ATBUS TIMINGS
OPTi Inc.
Size
A
Document Number
ATBUS1
REV
A.2
Date: October 1, 1991 Sheet 10 of 11


CLK2
ATCLK
HOLD
HLDA1
REF#
MEMRD#
IRQ
HLDA
t513
t514
t521
t522
t516
t517
t518
t519
t520
ATBUS HOLD TIMING
Note: HLDA1 is inactive during refresh cycle


t527
t528
NPBUSY#
NPERR#
NPINT
NPBUSY, NPERR TIMING


OPTi Inc.
Size
A
Document Number
ATBUS 2
REV
A.2
Date: October 1, 1991 Sheet 11 of 11


35.2±0.4
32.0±0.2
138
93
1.375TYP
139
92
32.0±0.2
35.2±0.4
184
47
1
46
1.375TYP
0.65
0.3±0.1
0.13 M
3.6±0.2
4.45MAX
0.1
33.6±0.4
0.45 +0.2 -0.1
0.15 +0.1 -0.05
0~10°
0.8±0.2